

WECON

Programming



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ABSD Instructions

1. Instruction Description

Name	Function	Bits(bits)	Pulse type	Instruction format	Step
ABSD	BIN addition operation	16	No	ABSD (S1) (S2) (D) (n)	9
DABSD		32	No		17

This instruction is a multi-section comparison, which is used for realizing cam control. The table and counter for comparison are all set in absolute mode. The instruction is implemented in the scanning main program, and the comparison result is affected by scan time delay.

Address:

(S1) is the starting component address of the comparison table.

(S2) is the counter component serial number. When using 32 bit instruction, it could be used as a 32 bit counter.

(D) is the starting address of the comparison result, occupying (n) several continuous bit variable units.

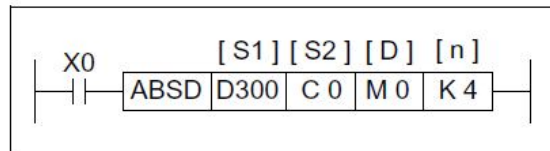
(n) is the number of multi-segment comparison data.

When using 32 bit instruction, (S1) (S2) (D) are all pointing to 32bit variable, and (n) is also calculated according to 32bit variable width.

Operand	Bit component				Word component										
	X	Y	M	S	K	H	KnX	KnY	KnM	KnS	T	C	D	V	Z
(S1)							✓	✓	✓	✓	✓	✓	✓		
(S2)												✓			
(D)				✓											
(n)	Constant,n = 1~64;														

When (S1) operands are KnX、KnY、KnM、KnS , if it is 16bit instruction, K4 must be specified; if it is 32bit instruction, K8 must be specified and the component number of X,Y,M,S must be a multiple of 8. (S1) operand can only specify C0 to C199 with 16bit instruction, and specify C200 to C254 with 32bit instruction.

2.Operation:



This instruction generates a variety of output patterns (there are n number of addressed outputs) in response to the current value of a selected counter, S2.

Points to note:

- The current value of the selected counter (S2) is compared against a user defined data table. This data table has a head address identified by operand S1. S1 should always have an even device number.
- For each destination bit (D) there are two consecutive values stored in the data table. The first allocated value represents the event number when the destination device (D) will be turned ON. The second identifies the

reset event. The data table values are allocated as a consecutive pair for each sequential element between D and D+n.

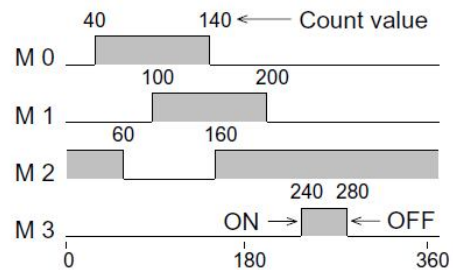
c) The data table has a length equal to $2 \times n$ data entries. Depending on the format of the data table, a single entry can be one data word such as D300 or a group of 16 bit devices e.g.K4X000.

d) Values from 0 to 32,767 may be used in the data table.

e) The ABSD instruction may only be used **ONCE**.

From the example instruction and the data table below, the following timing diagram for elements M0 to M3 can be constructed.

When counter S2 equals the value below, the destination device D is		Assigned destination device D
turned ON	turned OFF	
D300 - 40	D301 - 140	M0
D302 - 100	D303 - 200	M1
D304 - 160	D305 - 60	M2
D306 - 240	D307 - 280	M3



Instruction for use:

Before ABSD instruction is implemented, all the variables in the form should be assigned with a MOV instruction.

Even if the DABSD instruction is applied with high-speed instruction, the comparison result D[] is also affected by user program scan time delay. For the application with time response requirement, the HSZ high-speed comparison instruction is recommended.

3. PLC monitor

