

WECON

Programming



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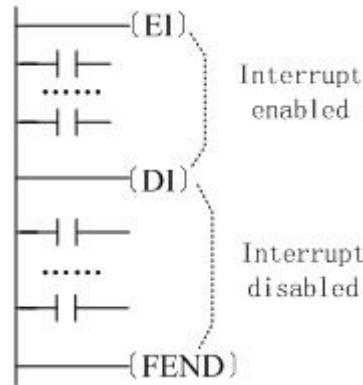
IRET, EI, DI Instructions

1. Instruction Description

Mnemonic	Function	Operands	Program steps
		D	
IRET FNC 03 (Interrupt return)	Forces the program to return from the active interrupt routine	N/A Automatically returns to the main program step which was being processed at the time of the interrupt call.	IRET: 1 step
EI FNC 04 (Enable interrupts)	Enables interrupt inputs to be processed	N/A Any interrupt input being activated after an EI instruction and before FEND or DI instructions will be processed immediately unless it has been specifically disabled.	EI: 1 step
DI FNC 05 (Disable interrupts)	Disables the processing of interrupt routines	N/A Any interrupt input being activated after a DI instruction and before an EI instruction will be stored until the next sequential EI instruction is processed.	DI: 1 step
I (Interrupt pointer)	Identifies the beginning of an interrupt routine	A 3 digit numeric code relating to the interrupt type and operation.	I☆☆☆: 1 step

Mnemonic	Function	Operands	Program steps
		D	
FEND (First end)	Used to indicate the end of the main program block	N/A Note: Can be used with CJ CALL and interrupt routines	FEND: 1 step

When PLC program is in operation, interruption is prohibited; after the execution of EI instruction, interruption function has become permissible; when DI instruction is executed during the permissible interruption status, the system enters the status of prohibitive interruption. In the programming, if there is no inter-zoning interruptive prohibition insertions, DI instruction cannot be executed.



Interrupt types and setting:

- 1) External signal input interrupts: they can be defined to trigger interrupts by rising or falling edges. For an X signal that doesn't need an immediate response, pulse capture function can also be used;
- 2) Timer interrupts: they occur every fixed period of 1ms~99ms.
- 3) High speed interrupts: they are used with DHSCS comparison setting instruction. Interrupt occurs when the present value of a high speed counter reaches the setting value.

External Signal Input Interruption Indication and Setup:

Input No.	Pointer No.		Interrupt disabled instruction
	Rising edge interrupt	Falling edge interrupt	
X000	I001	I000	M8050
X001	I101	I100	M8051
X002	I201	I200	M8052
X003	I301	I300	M8053
X004	I401	I400	M8054
X005	I501	I500	M8055

Timing Interruption Indicator and Setup:

Input No.	Interrupt period (ms)	Interrupt disable instruction
I6□□	Input 1~99 to □□ in the instructions, for example, I605, which executes one timing interrupt every 5 ms	M8056
I7□□		M8057
I8□□		M8058

High-speed interruption indicator and setup:

Input No.	Interrupt disable instruction
I010	M8059
I020	
I030	
I040	
I050	
I060	

Pulse Output Completion and Interruption Indicator and Setup: (the function requires the activation of M8090~M8094 in order to generate interruption after pulse output has been completed)

Port No.	Use special bit	Related user interrupts
Y000	M8090	I502
Y001	M8091	I503
Y002	M8092	I504
Y003	M8093	I505
Y004	M8094	I506

Interrupting sub-program uses different numbers to select different ports and interruption trigger edge;

External input interrupt can only be applied on same X, and it cannot be applied to both ascension and descension interrupting numbers at the same time. Only one trigger edge can be applied to one X input port. The trigger edge can be configured through indicator numbers.

External input interrupt: if M8050-M8055 is in the status of "ON" during the program execution process, the interruption function of the corresponding X port is prohibited.

Timing Interruption: if M8056-M8058 is in the status of "ON" during the program execution process, the interruption function of the corresponding X port is prohibited.

High-speed counter interruption: if M8059 is in the status of "ON" during the program execution process, the interrupting function of all the high-speed counters is prohibited.

Interruption instruction's programming requirements and execution features:

- Interruptions can be applied in between the D1 and E1 instructions (between the zones of prohibitive interruptions). The instruction can be saved in memory and later on executed after the EI instruction.
- Indicator number cannot be reused.
- When multiple interruptions are occurring in sequence, the prioritization is based on the sequence. When interruptions are happening all at the same time, the priority will base on it level of classification. The priorities from high to the low end are: high-speed counter, external, timing, pulse output completion.

- During the interruption execution process of regular programs, other interruptions are prohibited. However, if EI and DI instruction programs are being edited under the interruptive sub-programs, a maximum of two interruptions can be programmed.
- During the interruption process, both input and output relays can be controlled. By executing the input/output refresh instruction (REFF), the most current input status can be read, and the calculation results can be exported immediately to realize the task of high-speed control. For input relay numbers that are to be used by interruption indicator, please do not use numbers that are used in application instructions such as [high-speed counter] and [pulse density], which choose from the same input range.
- For the timer used in sub-programs and routine interruption programs, please use the T192-T199 timer specifically for the routine program. Should other regular timers be used, not only it cannot carry out the timing function, extra caution must be paid when using the 1ms cumulative timer.
- If the input interruption indicators, I and O ports, are designated, the input filter feature of the input relay will be automatically shut off. Therefore, it is unnecessary to use the REFE instruction and the special data register D8020 (input filter adjustment). Besides, the input filter of the input relay that is not being used by the input interruption indicator can maintain for 10ms (initial value).

In order to satisfy the operation of the high-speed counter, 30 additional high-speed counting interruptions are added. This allows any designated high-speed interruption to produce 30 interruption responses. The function is called "Multiple User-designated Interruption Feature" of high-speed counter. The operating configuration follows the following patterns:

Flag bit	description
M8084	Set to ON to enable high speed counter multi-user interrupts
D8084	High speed counter no. C235~C255
D8085	Related user interrupt numbers, 24 max from I507 to I530
D8086	Correspond to the serial numbers of several compare point data and can be used as D component only, such as 200, which represents a double word starting from D200.

Example of the Comparison Point Data Storage:

D8084=235;D8086=200;D8085=5;M8084=ON;

The data in C235	Recording unit	Save unit value	Related user interrupts	Value in D8131
100	D200, D201	=100	I507	0
200	D202, D203	=200	I508	1
300	D204, D205	=300	I509	2
400	D206, D207	=400	I510	3
500	D208, D209	=500	I511	4 → 0 (M8133=ON)

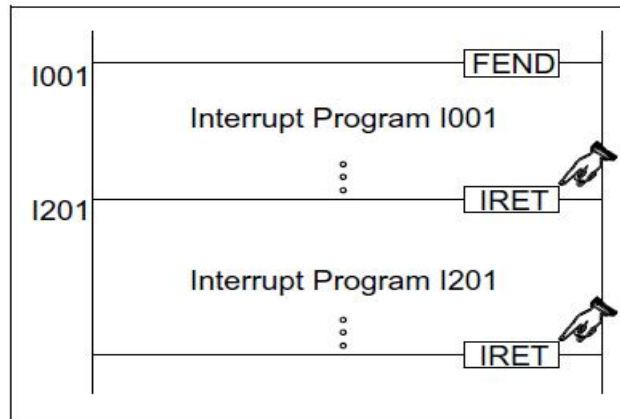
Every interruption can be produced by the values in the high-speed counter and the recorded units.

2.Operation:

Interrupts are triggered by different input conditions, sometimes a direct input such as X0 is used other times a timed interval e.g. 30 msec can be used. The availability of different interrupt types and the number operational points for each PLC type are detailed on page 2-5, Interrupt Pointers. To program and operate interrupt routines requires up to 3 dedicated instructions (those detailed in this section) and an interrupt pointer.

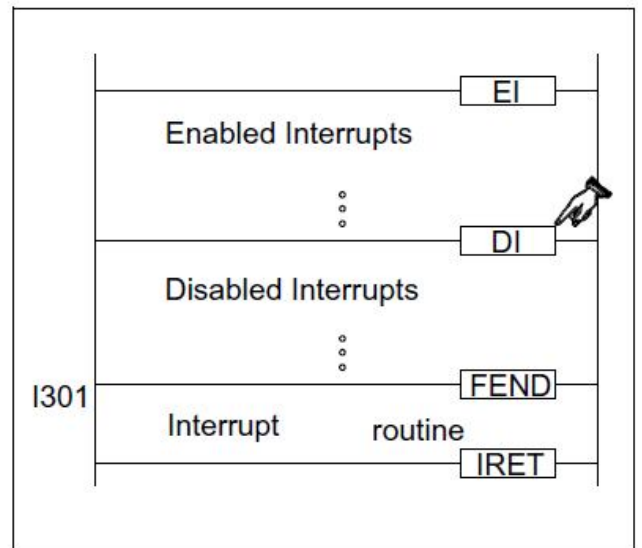
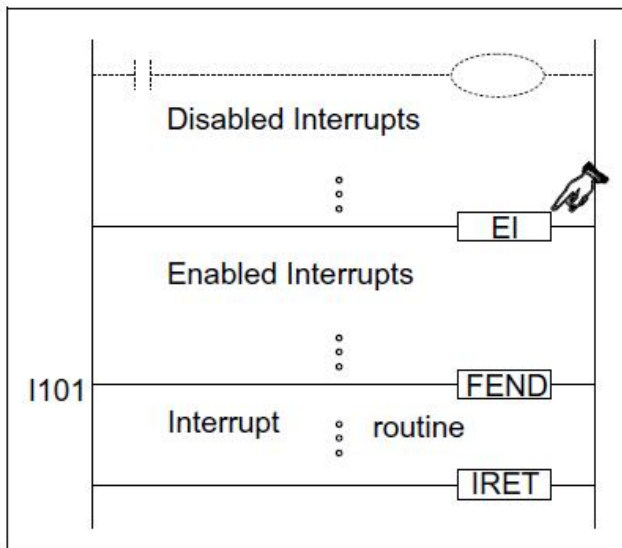
Defining an interrupt routine:

An interrupt routine is specified between its own unique interrupt pointer and the first occurrence of an IRET instruction. Interrupt routines are ALWAYS programmed after an FEND instruction. The IRET instruction may only be used within interrupt routines.



Controlling interrupt operations:

The PLC has a default status of disabling interrupt operation. The EI instruction must be used to activate the interrupt facilities. All interrupts which physically occur during the program scan period from the EI instruction until the FEND or DI instructions will have their associated interrupt routines run. If these interrupts are triggered outside of the enclosed range (EI-FEND or EI-DI, see diagram below) they will be stored until the EI instruction is processed on the following scan. At this point the interrupt routine will be run. If an individual interrupt is to be disabled its associated special M coil must be driven ON. While this coil is ON the interrupt routine will not be activated.



Nesting interrupts:

Interrupts may be nested for two levels. This means that an interrupt may be interrupted during its operation. However, to achieve this, the interrupt routine which may be further interrupted must contain the EI and DI instructions; otherwise as under normal operation, when an interrupt routine is activated all other interrupts are disabled.

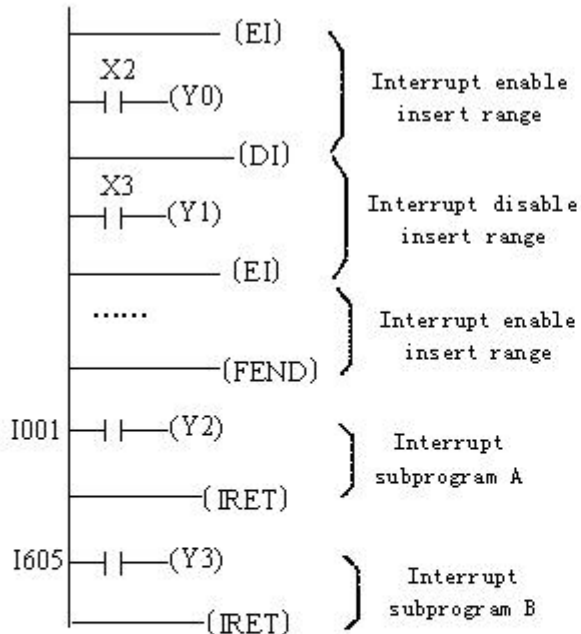
Simultaneously occurring interrupts:

If more than one interrupt occurs sequentially, priority is given to the interrupt occurring first. If two or more interrupts occur simultaneously, the interrupt routine with the lower pointer number is given the higher priority.

Using general timers within interrupt routines:

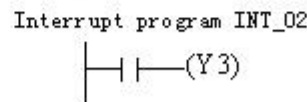
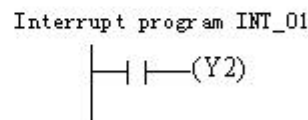
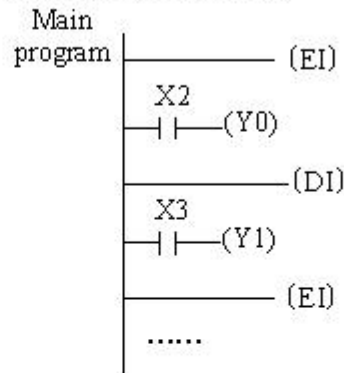
LX PLC's have a range of special timers which can be used within interrupt routines.

3.Program example:



In PLC operation, if the program between EI instruction and DI instruction is scanned or 5ms time is up, execute interrupt subprogram A or B; if the subprogram is executed to IRET, return to main program and continue to operation.

See the program in the left diagram in AutoShop: (right click the interrupt program INT_01 or INT_02 for this program and select attribute to rename it, including Chinese name)



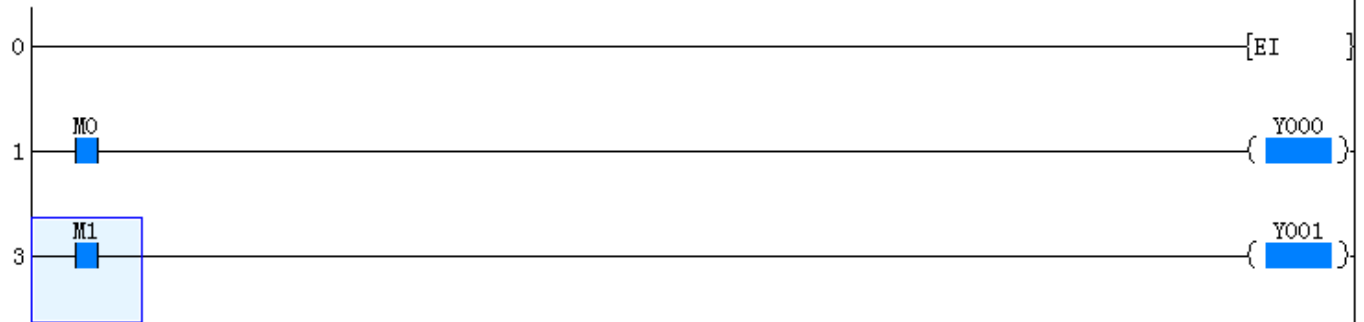
Right click interrupt program INT_01 and INT_02 for the program block and select attribute-interrupt items: set to I001 and I605 respectively

3.PLC monitor

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/*
 * IRET, EI, DI instruction
 */

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/*
 * If M8053=1, then x3 can not interrupt I301
 */

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